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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/874,173	06/04/2001	Spencer M. Gold	SMQ-043	7642

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/874,173	GOLD ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 2/8/2005.

Claim Objections

3. Claims 5 and 14 are objected to because of the following informalities: Applicant should clarify the claims because as currently worded, it seems as if each structure holds available registers, which the examiner believes is not the case. Instead, the first structure holds available registers, the second structure holds register assignments, and the third structure holds assignments after retirement of associated instructions. Appropriate correction is required.

Withdrawn Rejections

4. Applicant, via amendment, has overcome the rejections set forth in the previous Office Action. Consequently, those rejections are hereby withdrawn by the examiner. However, upon further consideration, a new grounds of rejection is applied below. Any or applicant's arguments associated with the previous rejections are considered moot.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-8, 10-12, and 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Yeager et al., U.S. Patent No. 5,758,112 (herein referred to as Yeager).

7. Referring to claim 1, Yeager has taught in a microprocessor having a plurality of physical registers, a method for managing said plurality of physical registers, said method comprising steps of:

a) providing a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor, said destination operand identifying where data resulting from an operation is to be stored. See Fig.2, component 210, and column 7, lines 40-42.

b) storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for an architectural register of a selected instruction executing on the microprocessor. See Fig.2, component 206, and column 7, lines 53-54. Note that the table holds the current register mappings.

c) transferring said physical register assignment of said selected physical register from said second structure to a third structure after retirement of said selected instruction, the third structure holding information regarding a plurality of physical register assignments. See Fig.2, component 212, and column 7, lines 54-57. Note that when a selected instruction is encountered,

a current register mapping associated with the instruction's destination register is stored in the mapping table, while the old mapping associated with that destination is sent to the active list. The instruction will eventually retire and the current mapping will still be in the mapping table. However, when a subsequent instruction uses the same destination after retirement of the selected instruction, the current mapping will become the old mapping and is moved to the active list. Therefore, it can be seen that after retirement of instructions, the mappings of those instructions will eventually be moved to the third structure (active list).

d) when said architectural register is assigned as a destination operand for a subsequent instruction, transferring information identifying said selected physical register as available from said third structure to said first structure. See column 8, lines 13-17.

8. Referring to claim 2, Yeager has taught a method as described in claim 1. Yeager has further taught the step of storing mappings of logical registers to said plurality of physical registers. See column 7, lines 40-42, and lines 50-54.

9. Referring to claim 3, Yeager has taught a method as described in claim 2. Yeager has further taught that the microprocessor is comprised of a memory array and wherein said method further comprises the step of storing said mappings to the memory array. See column 7, lines 53-54, and Fig.2, component 206. Note that a table is a memory array.

10. Referring to claim 5, Yeager has taught a method as described in claim 1. Yeager has further taught that contents of said first structure, second structure, and third structure of available registers are self-initialized to store mappings of said physical registers. See column 12, lines 24-50 and column 15, lines 61-63.

11. Referring to claim 6, Yeager has taught a method as described in claim 1. Yeager has further taught that contents of said assigned available physical registers are flushed from said assigned available physical registers. See column 15, lines 44-48, and note that when an exception occurs, the state of the system must be reversed. In doing this, results that have been written to registers will be flushed by restoring pre-exception assignments.

12. Referring to claim 7, Yeager has taught a method as described in claim 1. Yeager has further taught the step of detecting whether said assigned available physical registers are being utilized by said microprocessor for execution. If an available physical register is assigned to be a destination for an instruction, then that register is detected as being utilized during execution. That is, the processor will detect that register X is the destination and therefore, the result of the instruction will be written there.

13. Referring to claim 8, Yeager has taught a method as described in claim 1. Yeager has further taught that said method is performed by hardware. See Fig.2.

14. Referring to claim 10, Yeager has taught in a microprocessor having a plurality of physical registers, a method for managing said plurality of physical registers, said method comprising steps of:

a) providing a first structure for holding information identifying available physical registers that are free to be assigned to a plurality of destination operands for instructions executing on the microprocessor, said plurality of destination operands identifying where data resulting from an operation is to be stored. See Fig.2, component 210, and column 7, lines 40-42.

b) storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned to one of said plurality of destination operands for an architectural

register of a selected instruction executing on the microprocessor. See Fig.2, component 206, and column 7, lines 53-54. Note that the table holds the current register mappings.

c) providing a third structure for holding information regarding physical registers utilized during execution of instructions. See Fig.2, component 212, and column 7, lines 54-57.

d) transferring said physical register assignment of said selected physical register from said second structure to a third structure after retirement of said selected instruction. See Fig.2, component 212, and column 7, lines 54-57. Note that when a selected instruction is encountered, a current register mapping associated with the instruction's destination register is stored in the mapping table, while the old mapping associated with that destination is sent to the active list. The instruction will eventually retire and the current mapping will still be in the mapping table. However, when a subsequent instruction uses the same destination after retirement of the selected instruction, the current mapping will become the old mapping and is moved to the active list. Therefore, it can be seen that after retirement of instructions, the mappings of those instructions will eventually be moved to the third structure (active list).

e) when said architectural register is assigned as a destination operand for a subsequent instruction, transferring information identifying said selected physical register as available from said third structure to said first structure. See column 8, lines 13-17.

15. Referring to claim 11, Yeager has taught a method as described in claim 10. Furthermore, claim 11 is rejected for the same reasons set forth in the rejection of claim 2 above.

16. Referring to claim 12, Yeager has taught a method as described in claim 11. Furthermore, claim 12 is rejected for the same reasons set forth in the rejection of claim 3 above.

17. Referring to claim 14, Yeager has taught a method as described in claim 10. Furthermore, claim 14 is rejected for the same reasons set forth in the rejection of claim 5 above.

18. Referring to claim 15, Yeager has taught a method as described in claim 10. Furthermore, claim 15 is rejected for the same reasons set forth in the rejection of claim 6 above.

19. Referring to claim 16, Yeager has taught a method as described in claim 10. Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claim 7 above.

20. Referring to claim 17, Yeager has taught a method as described in claim 10. Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 8 above.

21. Referring to claim 19, Yeager has taught a microprocessor system with a plurality of physical registers for managing a plurality of physical register assignments comprising:

a) a first module for providing a first structure for holding information identifying available physical registers that are free to be assigned as a destination operand for instructions executing on the microprocessor, said destination operand identifying where data resulting from an operation is to be stored. See Fig.2, component 210, and column 7, lines 40-42.

b) a second module for storing a physical register assignment in a second structure noting that a selected one of the physical registers is assigned as a destination operand for an architectural register of a selected instruction executing on the microprocessor. See Fig.2, component 206, and column 7, lines 53-54. Note that the table holds the current register mappings.

c) a third module for providing a third structure for holding information regarding physical registers utilized during execution of instructions. See Fig.2, component 212, and column 7, lines 54-57.

d) a first interface for transferring said physical register assignment of said selected physical register from said second structure to said third structure after retirement of said selected instruction. See Fig.2, component 212, and column 7, lines 54-57. Note that when a selected instruction is encountered, a current register mapping associated with the instruction's destination register is stored in the mapping table, while the old mapping associated with that destination is sent to the active list. The instruction will eventually retire and the current mapping will still be in the mapping table. However, when a subsequent instruction uses the same destination after retirement of the selected instruction, the current mapping will become the old mapping and is moved to the active list. Therefore, it can be seen that after retirement of instructions, the mappings of those instructions will eventually be moved to the third structure (active list).

e) a second interface for, when said architectural register is assigned as a destination operand for a subsequent instruction, transferring information identifying said selected physical register as available from said third structure to said first structure. See column 8, lines 13-17.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 4, 13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeager, as applied above.

24. Referring to claim 4, Yeager has taught a method as described in claim 1. Yeager has not taught that said microprocessor simultaneously executes multiple threads. However, Official Notice is taken that threads and the ability of a processor to execute multiple threads in parallel (simultaneously) is well known and expected in the art. Threads are separate independent sections of code which perform a particular task. They are advantageous in that they hide the latency of a processor while performing a long-latency instruction such as a load from main memory. Instead of simply stalling and waiting for the result, the processor can switch to another thread and continue executing. In addition, when threads are executed in parallel, more work is being performed in a given amount of time, compared with executing a single thread at a time, serially. As a result, in order to increase the efficiency of the system, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yeager to execute multiple threads simultaneously.

25. Referring to claim 13, Yeager has taught a method as described in claim 10. Furthermore, claim 13 is rejected for the same reasons set forth in the rejection of claim 4 above.

26. Referring to claim 20, Yeager has taught a method as described in claim 19. Furthermore, claim 20 is rejected for the same reasons set forth in the rejection of claim 4 above.

27. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeager, as applied above, in view of Tanenbaum, Structured Computer Organization, 2nd Edition, 1984, page 11 (as applied in the previous Office Action and herein referred to as Tanenbaum).

28. Referring to claim 18, Yeager has taught a method as described in claim 1. Although Yeager has taught that said method is performed by hardware (Fig.2), Yeager has not explicitly

taught that said method is performed by software. However, Tanenbaum has taught that hardware and software are logically equivalent. See page 11. Therefore, a person of ordinary skill in the art would've recognized that the function performed by the hardware could be implemented in software and vice-versa. As Tanenbaum has further suggested, the choice between hardware and software implementations is based on the designer's needs as well as cost, speed, reliability, and frequency. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yeager such that software performs the method instead of hardware.

29. Referring to claim 18, Yeager has taught a method as described in claim 10. Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 9 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
April 20, 2005

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